Docket No.: M4065.0579/P579-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Alon Regev	(Divisional of 10/166,696 Filed June 12, 2002)
Application No.: New	Prior Group Art Unit: 2818
Filed: Concurrently herewith	Prior Examiner: L. Tran
For: REDUCING SIGNAL SWING IN A MATCH DETECTION CIRCUIT	

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached Form PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

The listed documents were cited in prior Application No. 10/166,696, filed June 12, 2002, from which this divisional application depends under 35 USC § 120.

While the information and references disclosed in this Information Disclosure Statement may be "material" pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

Application No.: New

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It is submitted that this Information Disclosure Statement is in compliance with 37 CFR § 1.98 and the Examiner is respectfully requested to consider the listed references.

Dated: April 20, 2004

Respectfully submitted,

By_____

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PTO/SB/08a/b (08-03)
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Substitute for form 1449A/B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	New
Filing Date	Concurrently Herewith
First Named Inventor	Alon Regev
Prior Art Unit	2818
Prior Examiner Name	L. Tran
Attorney Docket Number	M4065.0579/P579-A

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	6,101,115	08/2000	Ross	
	AB	6,240,001 B1	05/2001	Ross	
	AC	6,349,049 B1	02/2002	Schoy	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	AD	"Half-V_{DD} Bit-Line Sensing Scheme in CMOS DRAM's," Nicky Chau-Chun Lu et al., IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 4, August 1984, pp. 451-454	
	AE	"A 256M DRAM with Simplified Register Control for Low Power Self Refresh and Rapid Burn-in," Seung-Moon Yoo et al., 1994 Symposium on VLSI Circuits Digest of Technical Papers, pp. 85 and 86	
	AF	"Automatic Voltage-Swing Reduction (AVR) Scheme for Ultra Low Power DRAMs," Masaki Tsukude et al., 1994 Symposium on VLSI Circuits Digest of Technical Papers, pp. 87 and 88	
	AG	"A 250mV Bit-Line Swing Scheme for a 1V 4Gb DRAM," T. Inaba et al., 1995 Symposium on VLSI Circuits Digest of Technical Papers, pp. 99 and 100	

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